REMARKS

Examiner J. Diaz is thanked for a complete search and thorough Office Action.

Reconsideration of the objections to the drawings in Figs. 1 and 2 is respectfully requested for the following reasons.

Applicant has discovered that an incorrect sheet 1/4, containing Figs. 1 and 2, was submitted on filing of this Divisional application on Jan. 19, 2001. The correct sheet was submitted with our previous response, and is again submitted with this response, and should overcome the objection to the drawings, per the telephone conversation between the Examiner and the undersigned attorney on Sept. 4, 2002. (The enclosed Figures are identical to those filed with the parent application, now issued as U.S. Patent 6,211,050.) Withdrawal of the objection is so requested.

Reconsideration of the rejection of claims 18-19 under 35 U.S.C. 102(e) as being anticipated by Saitou et al. (U.S. Patent 5,739,546) based on new grounds for rejection is respectfully requested for the following reasons.

The applicant's invention is a structure for avoiding non-uniform polish-back in the kerf (scribe) area between chips.

Saitou et al. describe a method for making a ground line conductor 6, which is a first lead layer on a silicon oxide film 5, as shown in Fig. 3. Next, an insulating layer 7 is deposited on the silicon oxide film 5 and over the ground line conductor 6. Power supply lines 8 are formed from a second lead layer on the insulating layer 7 and over the ground line conductor 6, as shown in Fig. 3, and as described in col. 3, lines 3-18. Saitou's structure is not a patterned fill layer, as cited by the Examiner on page 3, line 6. Saitou's structure is a multilevel structure designed for burn-in and testing at a single level of metal interconnections, and does not serve as a single patterned fill layer for planarizing techniques. Saitou's structure does not anticipate the applicant's invention, and therefore the applicant's structure is non-obvious and patentable over Saitou et al.

Reconsideration of the rejection of claim 20 under 35 U.S.C. 103(a) as being unpatentable over Saitou et al. (U.S. Patent 5,739,546) in view of Lou (U.S. Patent No. 5,759,906) is respectfully requested for the following reasons.

Lou's patent is directed toward planarizing metal layers in the chip areas and does not address planarizing at the corners of the chips near the kerf area. Further, the dependent claim 20 does not stand on its own merit but is in support of the independent claim 18.

Reconsideration of the rejection of claims 21-22 under 35 U.S.C. 103(a) as being unpatentable over Saitou et al. (U.S. Patent 5,739,546) is respectfully requested for the following reasons.

Since Saitou et al. are making a multilevel metal structure intended for testing at a single metal level, and are not making a single patterned fill layer in the kerf area for that level, the applicant's structure is therefore non-obvious and patentable over Saitou et al. Further, claims 21 and 22 are dependent claims that do not stand on their own merits but are in support of independent claim 18.

It is requested that Examiner Jose R. Diaz call the undersigned Attorney at 845-452-5863 should there be anything that can be done to help bring this Patent Application to Allowance.

Respectfully submitted,

Stephen B. Ackerman

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